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DESIGN OF A LOW-LATENCY ROBUST ASYNCHRONOUS INTERFACE FOR GLOBALLY-ASYNCHRONOUS LOCALLY-SYNCHRONOUS (GALS) SYSTEMS

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Abstract: Contemporary digital systems must necessarily be based on the "System-on-Chip – SoC" concept. A natural implementation of SoC circuit uses global clock, but in DSM technology (Deep-Sub-Microm) global clock signal causes serious problems. An interesting style for SoC design that reduces the problems of the global clock is the GALS (Globally Asynchronous, Locally Synchronous) paradigm. Currently, the major drawback in the design of a GALS system, shows to be the asynchronous interface. The interface is of the type asynchronous wrapper (AWs), where the AWs found in literature are based on two controller ports that are asynchronous finite state machines. They are responsible for data communication between locally synchronous modules and are important in the performance of GALS systems. In addition, these ports are subject to essential hazard. This paper proposes a novel asynchronous wrapper based on a unique port controller aiming to the point-to-point GALS style and easily generalized to multi-point GALS systems. The proposed asynchronous wrapper allows the communication between modules to be performed in the two-phase handshake protocol, which reduces the latency time when compared to the previous ones, and is robust, the essential hazard. A comparison with seven wrappers found in literature shows that the proposed wrapper leads to an average reduction in latency time of 81% and average reduction in area of 83% in the FPGA (Field Programmable Gated Array) platform.