AN ARCHITECTURE FOR IMPLEMENTATION OF SELF-TIMED COMBINATIONAL DIGITAL CIRCUITS FOR LOW-POWER DESIGN

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Abstract: Digital circuit design demands critical requirements, such as power consumption, robustness, performance, etc, when it is implemented in VLSI (Very Large Scale Integration). The asynchronous paradigm presents interesting features aiming to solve for these critical requirements. An important class of the asynchronous paradigm is the so called QDI (Quasi Delay Insensitive) circuits that can also be used for critical requirements design. QDI circuits are interesting for critical applications because they are robust to noise, to temperature variations, to wire and gate delays and to supply voltage variation, having also low electromagnetic emissions. QDI combinational circuits are designed as a block of functions whose indicability shows the robustness of the circuit communication with the environment. This paper presents two architectures based on basic gates and an approach to the synthesis of the QDI functions blocks. The two new architectures were tested for a set of benchmarks and compared with the main architecture. Our proposal shows respectively a gain of up to 16.2%, 64.3%, 46.1% and 8.5% in time of latency, number of LUTs and power dynamic and static respectively.