CMOS INVERTER BASED VOLTAGE LEVEL SENSOR

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Abstract: This article presents a novel voltage level sensor, which reads a voltage and checks whether its value is above an upper limit Vmax, below a lower limit Vmin or between both limits. Because of its CMOS inverter based architecture, it shows the advantages of low area cost and low power consumption and is particularly useful for checking whether a capacitor is fully charged, fully discharged or in process of charge. All these advantages lead to potential practical applications when compared with the voltage sensors based on operational amplifiers, once the latter demands more transistors and thus more power. Circuit model, layout in TSMC 0.18 um technology and simulation results are presented.